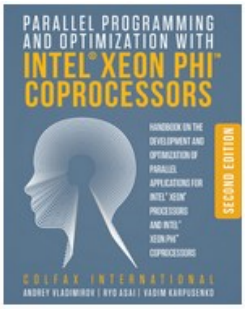
Parallel Programming and Optimization with Intel® Xeon Phi™ Coprocessors



Intel is offering an updated and expanded series of software developer trainings in parallel programming using the Intel® Xeon Phi™ coprocessors

This series of offerings provides software developers the foundation needed for modernizing their codes to extract more of the parallel compute performance potential found in both Intel® Xeon® processors and Intel Xeon Phi coprocessors.

The courses contain materials and practical exercises appropriate for developers beginning their journey to parallel programming, as well as provide cutting-edge detail to HPC experts on the best practices for Intel's multicore and many-core architectures and software development tools. The offerings includes a one-day introductory seminar (CDT 101, free) and hands-on laboratory (CDT 102, free).

The training targets software engineers and architects, and covers the following topics:

- Intel Xeon Phi architecture: purpose, organization, pre-requisites for good performance, future technology
- Programming models: native, offload, heterogeneous clustering
- Parallel frameworks: automatic vectorization, OpenMP, MPI
- Optimization methods: general, scalar math, vectorization, multithreading, memory access, communication and special topics

For more information and to register for a workshop in your area, use the QR code or visit:
http://tinyurl.com/2015ParallelProgrammingSeries

Event Details:
Date: Hybrid: October 13, 2015
Registration: 8:30 AM
Presentation: 9:00 AM to 4:00 PM
Location: University of Missouri
Locust Street Building
Room 205abc
615 Locust Street
Columbia, MO 65211

TRAININGS PRESENTED BY:

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**Cities are being continuously added, so check back often.*